IN THE CLAIMS

1. (Currently Amended) A system for instruction memory storage and processing in a computing device having a processor, the system being based on backwards branch control information, the system comprising:

a dynamic loop buffer (DLB) organized as a direct-mapped structure, said DLB being a tagless array of data;

a DLB controller having a primary memory unit partitioned into a plurality of banks, wherein said controller controls the state of the instruction memory storage system, accepts a program counter address (pc address) as an input, and outputs distinct signals;

an address register located in the memory of said computing device, wherein said address register is a staging register for said program counter address, and an instruction fetch process takes two cycles of said processor; and

a bank select unit for serving as a pc-address decoder to accept the program counter address and to output a bank enable signal for selecting a bank in a primary memory unit, and a decoded address for access within the selected bank, wherein the system is configured to:

fetch instruction packets from the primary memory unit,

write a copy of said instruction packets into the DLB,

set a valid bit to assert validity of said DLB,

enter an ACTIVE state when a backward branch is taken within a range of a loop,

enter an IDLE state when said backward branch completes a loop and a change